LISTING OF THE CLAIMS:

Claims 1-52 (Canceled)

53. (Previously presented) A dual workfunction high-performance support MOSFET/EDRAM array comprising at least one support region and at least one array region, said array region and said support region being separated by an isolation region, and at least a gate conductor guard ring formed around said array region on top of said isolation region, wherein said gate conductor guard ring prevents trapping of a stringer of gate conductor polysilicon on said isolation region.

54. (Previously presented) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 53 wherein said array region includes a plurality of DRAM cells embedded in a semiconductor substrate.

55. (Previously presented) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 54 wherein wordlines overlay each of said DRAM cells and a bitline overlays said wordlines.

56. (Original) The dual workfunction high-performance support MOSFET/EDRAM array of Claim 54 wherein each of said DRAM cells are vertical DRAMs.

Claims 57-59 (Canceled)